LAMPIRAN

BIDANG PENDIDIKAN DAN PENGAJARAN

BERITA ACARA PERKULIAHAN

PERIODE SEMESTER GENAP 2024/2025

MATA KULIAH:

Teknologi Rangkaian Terintegrasi

DAFTAR ISI :

PROGRAM STUDI TEKNIK ELEKTRO

FAKULTAS TEKNIK

INSTITUT SAINS DAN TEKNOLOGI NASIONAL

JAKARTA

YAYASAN PERGURUAN CIKINI
INSTITUT SAINS DAN TEKNOLOGI NASIONAL
Jl. Moh. Kahfi II, Bhumi Srengseng Indah, Jagakarsa, Jakarta Selatan 12640
Telp. 021-7270090 (hunting), Fax 021-7866955, hp: 081291030024
Email: humas@istn.ac.id Website: www.istn.ac.id

SURAT PENUGASAN TENAGA PENDIDIK

Nomor : 48-IV /03.1-F/III/2025

SEMESTER GENAP TAHUN AKADEMIK 2024/2025

Nama	: Ir. Irmayani, MT.	Status Pegawai	: Tetap
NIK/ NIDN/ NIDK	: 22900029/0310106501	Program Studi	: T.Elektro S1
Jabatan Akademik	: Lektor		

Bidang	Perincian Kegiatan	Tempat	Jam	Kredit (SKS)	Hari
I. PENDIDIKAN & PENGAJARAN	**1. Pengajaran di kelas termasuk laboratorium**				
	Teknologi Rangkaian Terintegrasi (kelas K)		18:00-20:50	3	Jum'at
	Sistem Komunikasi Serat Optik (kelas K)		17:00-18:40	1	Rabu
	Sistem Komunikasi Teristrial & Satelit (kelas K)		07:30-09:00	1	Sabtu
	MBKM 6 Bidang Manajemen (P)		19.00-20.40	2	Senin
	Piranti Gelombang Mikro (kelas K)		17.00-19.00	1	Senin
	2. Pembimbing				
	1. Seminar				
	2. Kerja Praktek				
	3. Tugas Akhir/Tesis			1	
	4. Pembimbing Akademik				
	3. Penguji				
	1. Tugas Akhir/Tesis				
	2. Kerja Praktek				
	4. Tugas Tambahan				
	1. Menduduki jabatan di Perguruan Tinggi				
II. PENELITIAN	1. Penelitian Ilmiah				
	2. Penulisan Karya Ilmiah			1	
	3. Penulisan Diktat Kuliah				
	4. Menerjemahkan Buku Kuliah				
	5. Pengembangan Program Kuliah Kurikulum				
	6. Pengembangan Bahan Ajar				
III. PENGABDIAN PADA MASYARAKAT	1. Menduduki jabatan di Pemerintahan				
	2. Pengembangan Hasil Pendidikan dan Penelitian				
	3. Memberikan penyuluhan/pelatihan/penataran/ceramah			1	
	4. Memberikan Pelayanan Kepada Masyarakat				
	5. Menulis karya Pengmas yang tidak dipublikasikan				
	6. Pengelolaan Jurnal Ilmiah				
IV. PENUNJANG	1. Menjadi anggota/panitia pada badan/lembaga suatu PT				
	2. Menjadi anggota Badan Lembaga Pemerintah				
	3. Menjadi anggota organisasi profesi				
	4. Mewakili PT/lembaga pemerintah, duduk dalam panitia antar lembaga				
	5. Menjadi anggota delegasi nasional ke pertemuan internasional				
	6. Berperan Serta Aktif dalam pertemuan ilmiah/seminar			1	
	7. Anggota dalam tim layanan pendidikan				
Jumlah Total				12	

Kepada yang bersangkutan akan diberikan gaji/honorarium sesuai dengan peraturan penggajian yang berlaku di Institut Sains dan Teknologi Nasional. Penugasan ini berlaku dari tanggal 01 Maret 2025 sampai dengan 31 Agustus 2025

Jakarta, 01 Maret 2025

Dr. Ir. Suryawan Murtiadi, MT
NIP. 4451

Tembusan :
1. Wakil Rektor 1 - ISTN
2. Wakil Rektor 2 - ISTN
3. Ka. Biro Sumber Daya Manusia - ISTN
4. Arsip

INSTITUT SAINS DAN TEKNOLOGI NASIONAL

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Website : www.istn.ac.id / e-Mail : admin@istn.ac.id / Telepon : (021) 7270090

JURNAL PERKULIAHAN
TEKNIK ELEKTRO 2024 GENAP

MATA KULIAH : Teknologi Rangkaian Terintegrasi
NAMA DOSEN : Ir. IRMAYANI, MT.
KREDIT/SKS : 3 SKS
KELAS : K

TATAP MUKA KE	HARI/TANGGAL	MULAI	SELESAI	RUANG	STATUS	RENCANA MATERI	REALISASI MATERI	KEHADIRAN MHS	PENGAJAR	TANDA TANGAN
1	Sabtu, 22 Maret 2025	10:00	12:00		Selesai	PENDAHULUAN	Terlaksana	(10 / 15)	Ir. IRMAYANI, MT.	
2	Jumat, 28 Maret 2025	15:00	15:30		Selesai	Perkembangan Integrated Circuit	Terlaksana	(10 / 15)	Ir. IRMAYANI, MT.	
3	Kamis, 10 April 2025	21:00	22:00		Selesai	Teknologi wafer: czochralski, Float Zone, Bridgman	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
4	Kamis, 17 April 2025	21:00	22:00		Selesai	Epitaksi	Terlaksana	(15 / 15)	Ir. IRMAYANI, MT.	
5	Rabu, 23 April 2025	10:50	12:20		Selesai	Oksidasi	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
6	Jumat, 25 April 2025	18:00	20:50		Selesai	Difusi	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
7	Jumat, 9 Mei 2025	21:00	22:10		Selesai	Fotolitografi	Terlaksana	(12 / 15)	Ir. IRMAYANI, MT.	
8	Kamis, 15 Mei 2025	13:10	15:00		Selesai	UTS	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
9	Jumat, 30 Mei 2025	13:00	15:20		Selesai	Proses pabrikasi Transistor dalam IC	Terlaksan	(0 / 15)	Ir. IRMAYANI, MT.	
10	Jumat, 13 Juni 2025	13:00	15:20		Selesai	Perancangan IC analog (Perancangan sederhana rangkaian penguat transistor BJT)	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
12	Jumat, 20 Juni 2025	13:30	15:40		Selesai	Pengantar CMOS	Terlaksan	(0 / 15)	Ir. IRMAYANI, MT.	
11	Selasa, 1 Juli 2025	21:00	22:00		Selesai	Perancangan rangkaian sederhana dalam IC	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
13	Jumat, 4 Juli 2025	13:00	15:30		Selesai	Fabrikasi Gerbang Logika CMOS (NAND, NOR Gate)	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	
14	Jumat, 11 Juli 2025	18:00	20:50		Selesai	Perancangan Layout NAND, NOR, NOT	Terlaksana Bahan pembelajaran yang telah dibagikan adalah Perancangan dgn Diagram Stik	(0 / 15)	Ir. IRMAYANI, MT.	
15	Jumat, 18 Juli 2025	18:00	20:50		Selesai	Perancangan rangkaian logika CMOS (IC DIGITAL)	Terlaksana Bahan pembelajaran yang telah dibagikan adalah TUGAS III RANCANGAN LAYOUT	(10 / 15)	Ir. IRMAYANI, MT.	
16	Sabtu, 2 Agustus 2025	18:00	20:50	R-C1	Selesai	UAS	Terlaksana	(0 / 15)	Ir. IRMAYANI, MT.	

Jakarta, 08 Agustus 2025
Ketua Prodi Teknik Elektro

Dr._ing. AGUS SOFWAN, M.Eng.Sc.
NIDN 0331076204

INSTITUT SAINS DAN TEKNOLOGI NASIONAL

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LAPORAN PERSENTASE PRESENSI MAHASISWA
TEKNIK ELEKTRO
2024 GENAP

Mata kuliah : Teknologi Rangkaian Terintegrasi
Nama Kelas : K
Dosen Pengajar : Ir. IRMAYANI, MT.

No	NIM	Nama	Pertemuan	Alfa	Hadir	Ijin	Sakit	Presentase
Peserta Reguler								
1	23224501	EUNIKE NATALIA WAROY	16	1	15			93.75
2	23224714	AULIA PARDAMEAN ARITONANG	16		16			100
3	23224715	ARIF MAULANA	16	1	15			93.75
4	23224717	FERI PAKPAHAN	16		16			100
5	23224718	CHRISTIANI SITINJAK	16		16			100
6	23224720	MUHAMMAD SAYUDI PUTRA	16	3	13			81.25
7	24220701	Ibrahim Abdul Hafizh	16	15	1			6.25
8	24224702	Km Chandra Bayu Saputra	16	1	13	2		81.25
9	24224703	Akbar Rhamadan	16		14	1	1	87.5
10	24224705	Muhammad Rafi	16		15	1		93.75
11	24224707	Melisa Aftantia	16		16			100
12	24224716	Alisa	16	2	13	1		81.25
13	24224718	M. Rafsanjani	16	12	4			25
14	24224725	M. FARIS FALAHUDIN	16	2	14			87.5
15	24224727	AYUDITA RIZKY ALDWITANTI	16	2	14			87.5

Jakarta, 12 Agustus 2025
Ketua Prodi Teknik Elektro

Dr._ing. AGUS SOFWAN, M.Eng.Sc.
NIP. 198509-008

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Jl. Moch. Kahfi II No.RT.13, RT.13/RW.9, Srengseng Sawah, Kec. Jagakarsa, Kota Jakarta Selatan, DKI Jakarta
Website : www.istn.ac.id / e-Mail : admin@istn.ac.id / Telepon : (021) 7270090

LAPORAN NILAI PERKULIAHAN MAHASISWA
Program Studi S1 Teknik Elektro
Periode 2024 Genap

Mata kuliah : Teknologi Rangkaian Terintegrasi
Nama Kelas : K
Kelas / Kelompok :
Kode Mata kuliah : EL1614
SKS : 3

No	NIM	Nama Mahasiswa	TUGAS INDIVIDU (20,00%)	UTS (30,00%)	UAS (40,00%)	KEHADIRAN (10,00%)	Nilai	Grade	Lulus	Sunting KRS?	Info
1	23224501	EUNIKE NATALIA WAROY	60.00	65.00	65.00	75.00	65.00	B-	✓		
2	23224714	AULIA PARDAMEAN ARITONANG	70.00	70.00	65.00	100.00	71.00	B	✓		
3	23224715	ARIF MAULANA	55.00	70.00	65.00	90.00	67.00	B-	✓		
4	23224717	FERI PAKPAHAN	80.00	70.00	65.00	90.00	72.00	B+	✓		
5	23224718	CHRISTIANI SITINJAK	65.00	65.00	65.00	100.00	68.50	B	✓		
6	23224720	MUHAMMAD SAYUDI PUTRA	50.00	70.00	65.00	90.00	66.00	B-	✓		
7	24220701	Ibrahim Abdul Hafizh	0.00		0.00		0.00	E			
8	24224702	Km Chandra Bayu Saputra	65.00	65.00	65.00	80.00	66.50	B-	✓		
9	24224703	Akbar Rhamadan	75.00	75.00	70.00	100.00	75.50	A-	✓		
10	24224705	Muhammad Rafi	70.00	75.00	70.00	80.00	72.50	B+	✓		
11	24224707	Melisa Aftantia	85.00	70.00	75.00	100.00	78.00	A-	✓		
12	24224716	Alisa	75.00	70.00	75.00	100.00	76.00	A-	✓		
13	24224718	M. Rafsanjani	0.00		0.00	75.00	7.50	E			
14	24224725	M. FARIS FALAHUDIN	75.00	70.00	70.00	75.00	71.50	B	✓		
15	24224727	AYUDITA RIZKY ALDWITANTI	75.00	70.00	70.00	85.00	72.50	B+	✓		

Tanggal Cetak : Sabtu, 9 Agustus 2025, 17:14:11

Paraf Dosen :

Ir. IRMAYANI, MT.

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DAFTAR HADIR UAS (UAS)

Program Studi : S1 - Teknik Elektro
Periode Akademik : 2024 Genap
Jadwal : -
Mata Kuliah : EL1614 - Teknologi Rangkalan Terintegrasi
Nama Kelas : K
Kelompok : -

NO	NIM	NAMA	TANDA TANGAN	
1	23224501	EUNIKE NATALIA WAROY	1	
2	23224714	AULIA PARDAMEAN ARITONANG		2
3	23224715	ARIF MAULANA	3	
4	23224717	FERI PAKPAHAN		4
5	23224718*	CHRISTIANI SITINJAK	5	
6	23224720	MUHAMMAD SAYUDI PUTRA		6
7	24220701*	Ibrahim Abdul Hafizh	7	
8	24224702	Km Chandra Bayu Saputra		8
9	24224703	Akbar Rhamadan	9	
10	24224705	Muhammad Rafi		10
11	24224707	Melisa Aftantia	11	
12	24224716*	Alisa		12
13	24224718*	M. Rafsanjani	13	
14	24224725*	M. FARIS FALAHUDIN		14
15	24224727*	AYUDITA RIZKY ALDWITANTI	15	

Keterangan, mahasiswa tidak dapat mengikuti ujian karena :

* : Memiliki tanggungan keuangan (tagihan).

Jakarta, 2-8-2025

Irmayani

Teknologi Rangkaian Terpadu

Irmayani

20 Steps of CMOS Fabrication Process

The CMOS can be fabricated using different processes such as:

- N-well process for CMOS fabrication
- P-well process
- Twin tub-CMOS-fabrication process

The fabrication of CMOS can be done by following the below shown twenty steps, by which CMOS can be obtained by integrating both the NMOS and PMOS transistors on the same chip substrate. For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs are required in which semiconductor type and substrate type are opposite to each other.

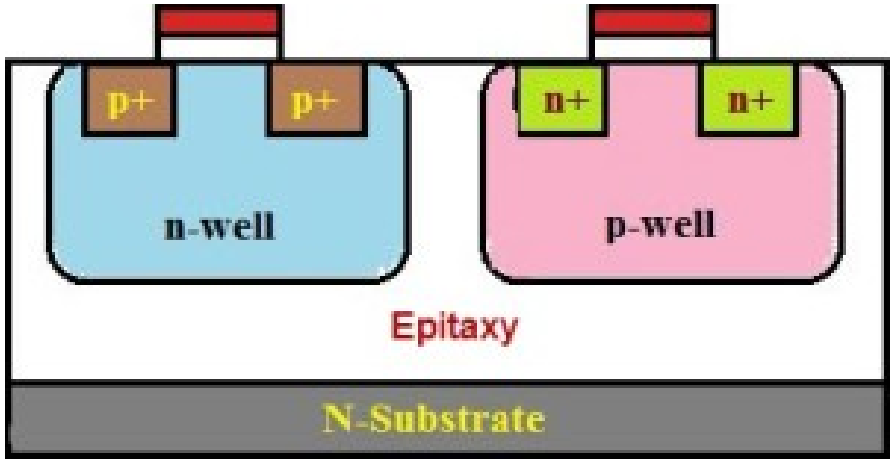
A P-well has to be created on a N-substrate or N-well has to be created on a P-substrate. In this article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.

The fabrication process involves twenty steps, which are as follows:

Fabircation of CMOS using P-well process

Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS. P-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices.

Twin tub-CMOS Fabrication Process



In this process, separate optimization of the n-type and p-type transistors will be provided. The independent optimization of Vt, body effect and gain of the P-devices, N-devices can be made possible with this process.

Different steps of the fabrication of the CMOS using the twintub process are as follows:

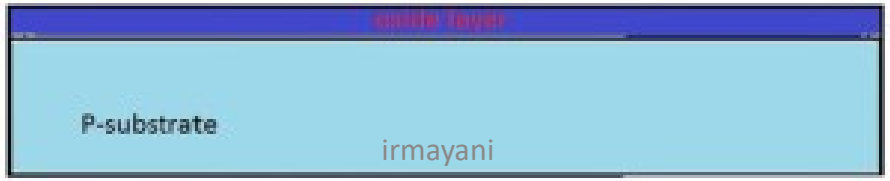
The fabrication process involves twenty steps, which are as follows:

Step1: Substrate

Primarily, start the process with a P-substrate.

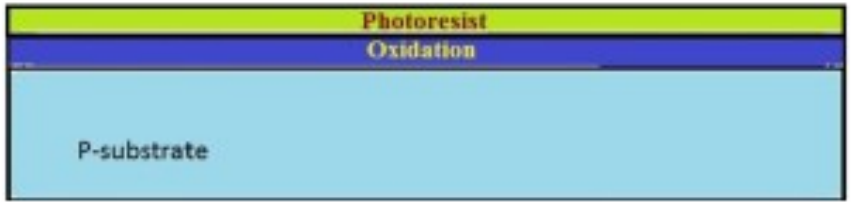
Step2: Oxidation

The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.



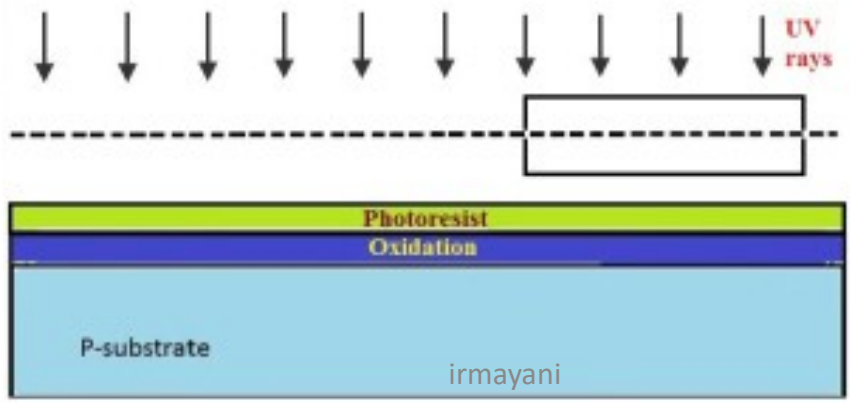
Step3: Photoresist

A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.



Step4: Masking

The photoresist is exposed to UV rays through the N-well mask

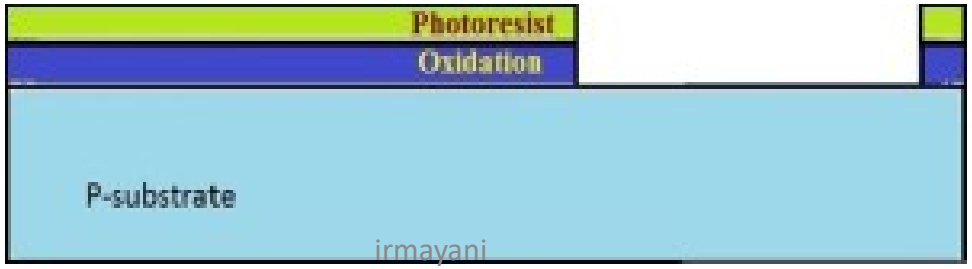


Step5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.

Step6: Removal of SiO2 using acid etching

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.



Step7: Removal of photoresist

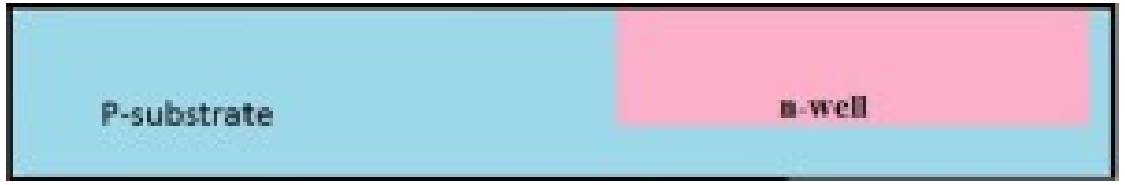
The entire photoresist layer is stripped off, as shown in the below figure.

Step8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.

Step9: Removal of SiO2

Using the hydrofluoric acid, the remaining SiO2 is removed.

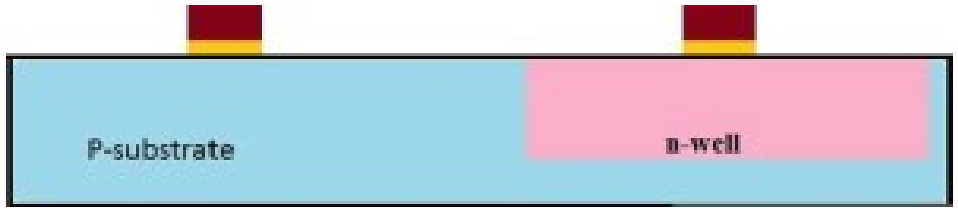


Step10: Deposition of polysilicon

Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.

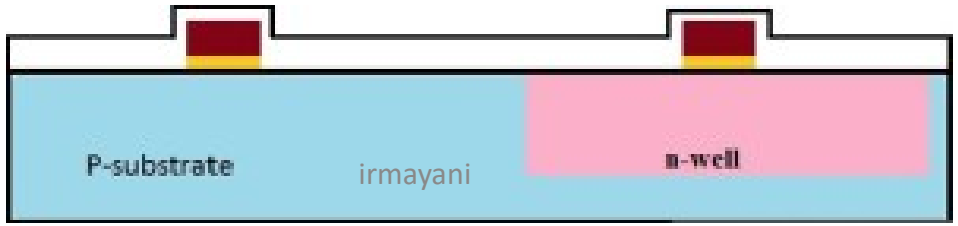
Step11: Removing the layer barring a small area for the Gates

Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



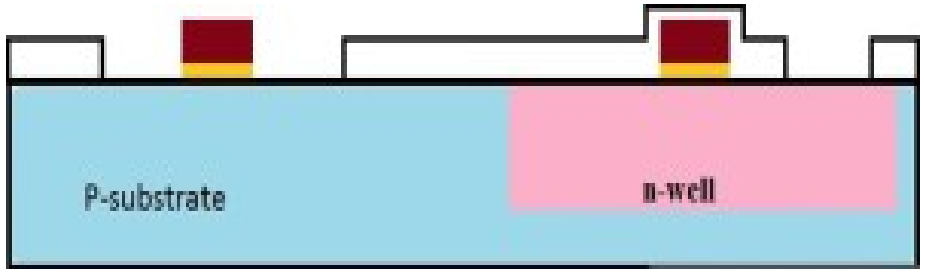
Step12: Oxidation process

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.

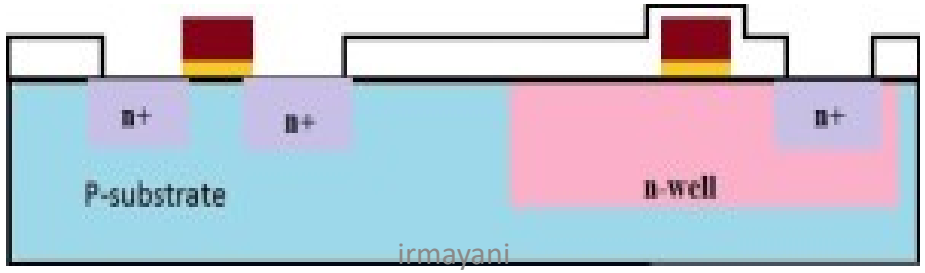


Step13: Masking and N-diffusion

By using the masking process small gaps are made for the purpose of N-diffusion.



The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.

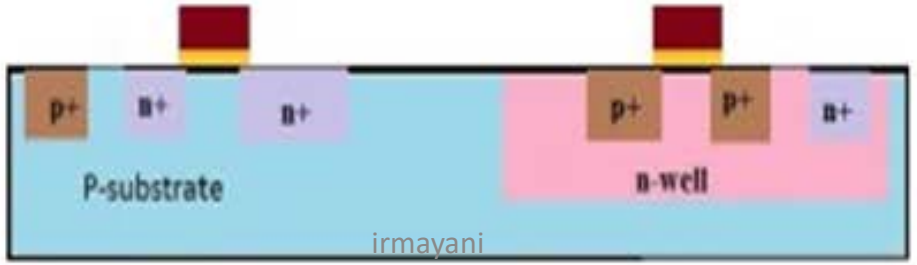


Step14: Oxide stripping

The remaining oxidation layer is stripped off.

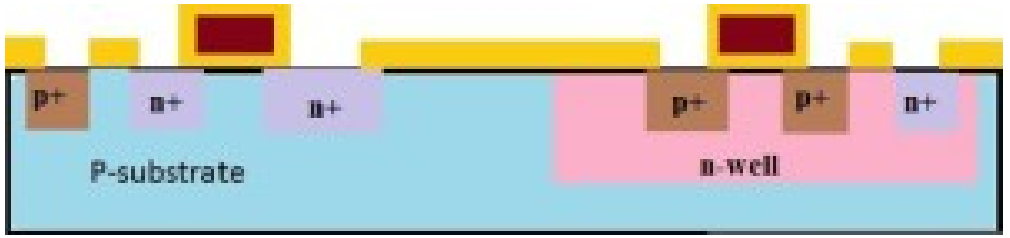
Step15: P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



Step16: Thick field oxide

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.

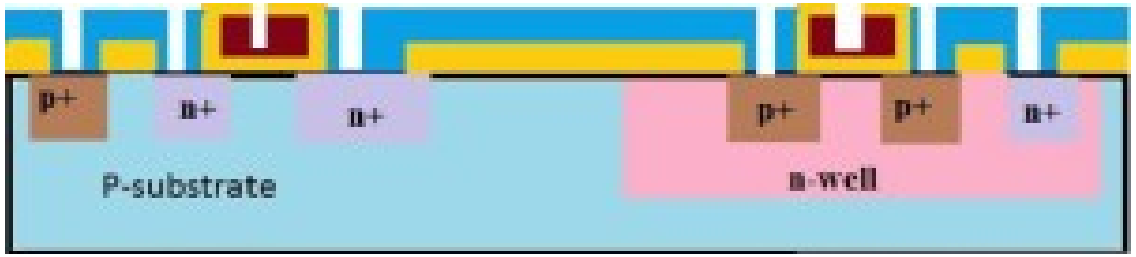


Step17: Metallization

Aluminum is sputtered on the whole wafer.

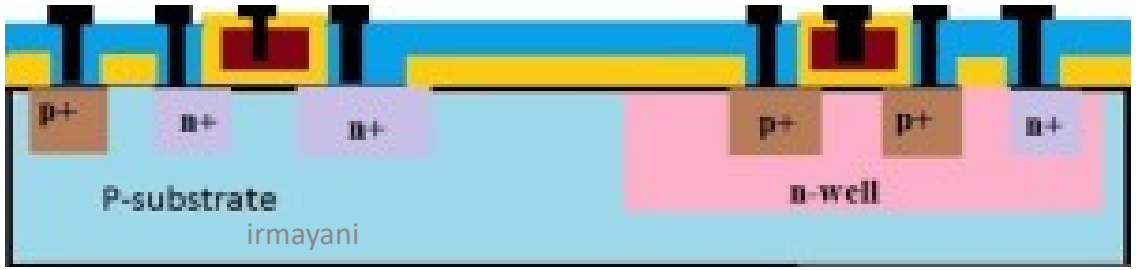
Step18: Removal of excess metal

The excess metal is removed from the wafer layer.



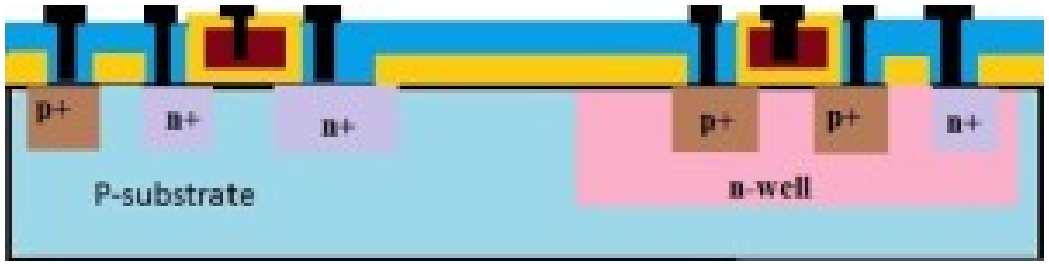
Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.



Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.



Step20: Assigning the names of the terminals of the NMOS and PMOS